3N153
T-31-25

Silicon Insulated-Gate Field-Effect Transistor

For Chopper and Multiplex Service in Communications, Navigation, and Instrumentation Equipment and in Industrial Control Circuits

Features:

- *Excellent thermal stability*
- *Virtually zero inherent offset voltage*
- *Low leakage current: 50 pA max.*
- *Low "on" resistance—$r_{DS(on)}$ = 200Ω typ.*
- *High "off" resistance—$R_{DS(off)}$ = 10^{10}Ω typ.*
- *Low feedback capacitance—C_{rss} = 0.34 pF typ.*
- *Low input capacitance—C_{iss} = 6 pF typ.*

Applications:

- *Choppers*
- *Multiplexers*
- *Servo Amplifiers*
- *Computer Operational Amplifiers*
- *Sampling Circuits*
- *Electrometer Amplifiers*

RCA 3N153• is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60 MHz.

The insulated gate provides a very high value of input resistance (10^{10} ohms typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N153 also features extremely low feedback capacitance (0.34pF typ.) and virtually zero inherent offset voltage.

This transistor features a Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The 3N153 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

• Formerly Dev. No. TA7352.

* Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values:*

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max. V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+20, −0.3 max. V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+20, −0.3 max. V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	+6, −8 max. V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max. V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50 max. mA
TRANSISTOR DISSIPATION, P_T:	
At ambient temperatures	
from −65 to +25°C	400 max. mW
above 25°C	derate linearly at 2.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Storage	−65 to +175°C
Operating	−65 to +175°C
LEAD TEMPERATURE	
(During soldering):	
At distance ≥ 1/32" to seating surface for 10 seconds max.	265 max. °C

3N153

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N153			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 25°C V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 125°C	- -	0.1 -	50 1	pA nA
Static Drain-to-Source "ON" Resistance	$r_{DS(on)}$	V_{GS} = 0V, V_{DS} = 0V	-	200	300	Ω
Drain-to-Source "OFF" Resistance	$R_{DS(off)}$	V_{GS} = -8V, V_{DS} = +1V	10^9	10^{10}	-	Ω
Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{GS} = -8V, V_{DS} = +1V, T_A = 25°C V_{GS} = -8V, V_{DS} = +1V, T_A = 125°C	- -	0.1 0.1	1 1	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz V_{DS} = 15V, I_D = 5 mA, f = 1 MHz	- -	0.34 0.12	0.5 0.2	pF pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz	-	6	8	pF
Small-Signal, Drain-to-Source Capacitance	C_{ds}	V_{DS} = 0V, V_{GS} = -8V, f = 1 MHz	-	-	3	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{GS} = 0V, V_{DS} = +15V	-	10,000	-	μmho
Offset Voltage	V_o	V_{GS} = +6,-8V; V_{DS} = 0V	-	0*	-	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No.107-1.0.1, or equivalent.

OPERATING CONSIDERATIONS

The flexible leads of the 3N153 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device.

TYPICAL CHARACTERISTICS

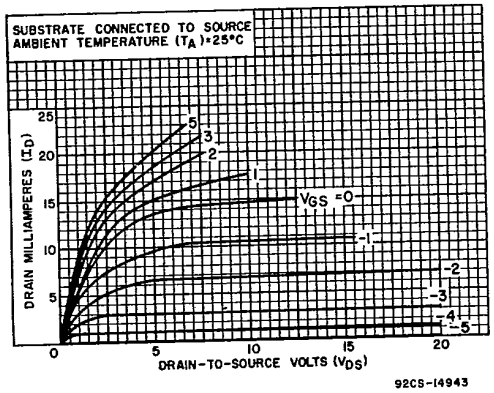


Fig.1 - Drain current vs. drain-to-source voltage.

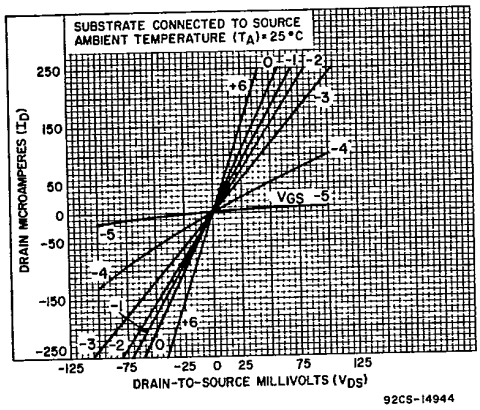


Fig.2 - Low-level drain current vs. drain-to-source voltage.

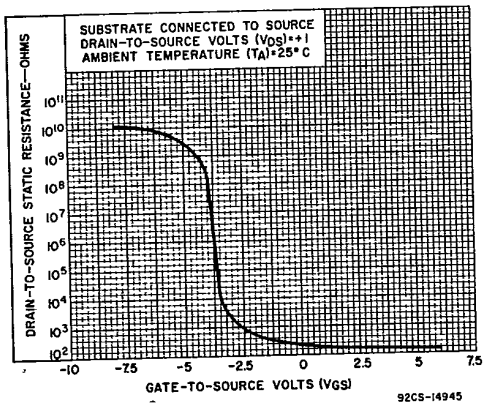
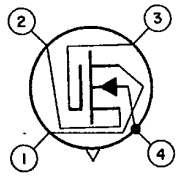


Fig.3 - Drain-to-source static resistance vs. gate-to-source voltage.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case